Japanese Journal of Applied Physics **51** (2012) 064101 **REGULAR PAPER**
DOI: 10.1143/JJAP.51.064101

Controllable Crystallization in Phase-Change Memory for Low-Power Multilevel Storage

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Received February 24, 2012; accepted March 18, 2012; published online May 15, 2012

We report current-driven crystallization in a $TiSi_3/Ge_2Sb_2Te_5/TiN$ vertical cell, which can be well controlled and is expected to be applied to multilevel storage with a low threshold voltage of about 1 V. We demonstrate that the number of distinct resistance levels can readily reach 8 and even higher. These levels in this study result from the initial threshold switching and the subsequent current-controlled crystallization induced by Joule heating. The latter allows the creation of many distinct levels, thus enabling the low-cost ultrahigh-density nonvolatile memory.

1. Introduction

Today's explosive proliferation of information requires more and more nonvolatile memory (NVM), which can stably store information even if no power is supplied.[1–5] To store more information, researchers have focused their attention on multilevel storage (MLS), which is data storage of more than two levels per memory cell.[6–9] It makes a dramatic increase in memory capacity possible, i.e., much more information can be stored without increasing the cell size.

In recent years, MLS has been demonstrated in both conventional and emerging memories, such as flash memory,[10] phase-change memory (PCM),[11,12] and resistive random access memory (RRAM).[13] However, flash memory itself has many demerits, such as a long write/erase time, low endurance, high programming energy, high programming voltage, and limited scalability.[14] The mechanism of RRAM is still not understood very well, so it will be difficult to obtain stable MLS for RRAM.[15]

PCM is based on reversible phase transformation between amorphous and crystalline phases with a huge resistance change. High power is required for amorphization since the phase change material must be heated above its melting point [e.g., 635 °C for $Ge_2Sb_2Te_5$ (GST)]. On the other hand, the crystallization proceeds at a low temperature (e.g., 150 °C for GST).

There are some reports of MLS based on multilayer structures[16,17] or the properties of phase-change materials with different phase-change temperatures.[18,19] However, the available number of resistance levels is strictly dependent on the number of multilayers or the phase-change temperatures. For example, only four resistance levels corresponding to two bits can be obtained with three phase-change layers or three different phase-change temperatures. Eight resistance levels become extremely difficult to be obtained because seven phase-change layers are necessary by adopting multilayer structures for MLS. Similarly, almost no phase-change materials exist with seven different phase-change temperatures.

On the other hand, although MLS with more than eight resistance levels was demonstrated by some groups such as IBM based on high-power amorphization,[20] there is a lack of study on MLS based on low-power crystallization. In this study, we report the control of resistance realized mainly through the gradual enlargement of the crystallization region induced by current-driven Joule heating using a vertical $TiSi_3/Ge_2Sb_2Te_5$ (GST)/TiN structure and eight resistance levels are demonstrated using this method.

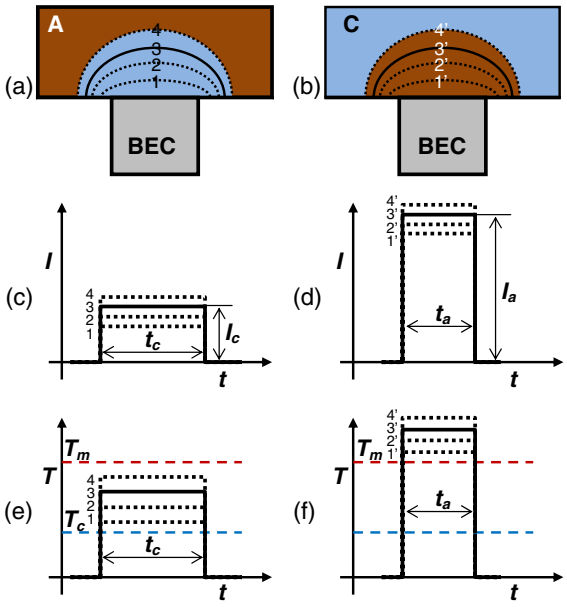

Fig. 1. (Color online) Approaches to multilevel storage. (a) Cross section of a device where the promotion of crystallization is shown. (b) Cross section of a device where the promotion of amorphization is shown. (c) Low electric pulses with different amplitudes for inducing crystallization regions of different sizes. (d) High electric pulses with different amplitudes for inducing amorphization regions of different sizes. (e) Different temperature profiles during application of crystallization-induced pulses. T_m and T_c are the melting point and crystallization temperature of the phase-change material, respectively. (f) Different temperature profiles during application of amorphization-induced pulses.

2. Comparison of MLS Concepts

The principle of PCM was simply introduced above. As we can see, MLS can be realized based on crystallization and amorphization in theory, as shown in Figs. 1(a) and 1(b), respectively. When a low but long electrical pulse with a width of t_c and an amplitude of I_c, as shown in Fig. 1(c), is applied to heat a chalcogenide phase-change alloy to a temperature between the melting point (T_m) and the crystallization temperature (T_c) of the alloy, as shown in Fig. 1(e), the chalcogenide alloy layer would be crystallized, and thus, a lowly resistive crystalline state could be written into the cell. The crystallized region is strongly dependent on the amplitude of the applied pulse. Intermediate resistance levels corresponding to different crystallized regions [e.g., regions

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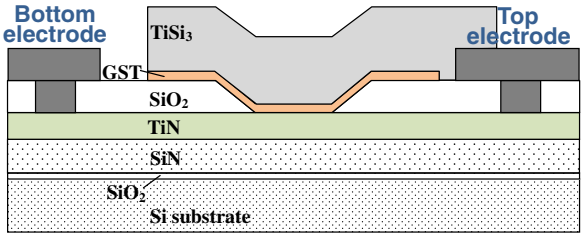

Fig. 2. (Color online) Cross-sectional structure of the multilevel storage phase-change memory device with a $TiSi_3/Ge_2Sb_2Te_5/TiN$ vertical structure.

with 1, 2, 3, or 4 outlines as shown in Fig. 1(a)] are available simply by applying different voltage pulses. On the other hand, by applying a high but short electrical pulse, as shown in Fig. 1(d), to a PCM cell, the chalcogenide alloy is heated to a temperature above T_m, as shown in Fig. 1(f), and then the melted part is quenched below T_c so quickly that crystallization can be sufficiently prevented. The PCM cell then enters a highly resistive amorphous state. Similarly to crystallization, the amorphized region [e.g., regions with 1′, 2′, 3′, or 4′ outlines as shown in Fig. 1(b)] is also controllable by applying different pulses. These different amorphized regions correspond to different resistance levels. The crystallization temperature of chalcogenide alloy (150 °C for GST) is much lower than its melting point (635 °C for GST). Reported experimental results also showed that the necessary current for crystallization is typically about 1/6–1/3 of that for amorphization, where pulses with the same width were used for both crystallization and amorphization.[21–23] Thus, the necessary power for crystallization is much lower than that for amorphization. Here, we focus on the crystallization-based MLS, which is characterized by low power as described above.

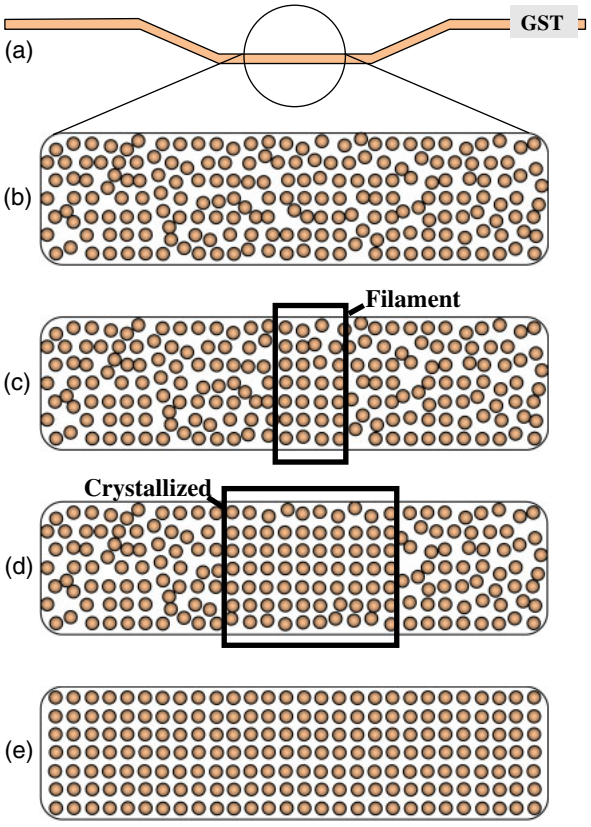

Fig. 3. (Color online) Mechanism of multilevel storage of the device in this work. (a) GST layer. (b) Amorphous phase with the highest resistance level. (c) Filament formation causing the drop of device resistance to an intermediate-resistance level by applying a current higher than the threshold current corresponding to the threshold voltage. (d) Crystallization causing the drop of device resistance to an intermediate-resistance level by applying an increasing current. (e) Complete crystallization causing the drop of device resistance to the lowest resistance level by applying a sufficiently high current.

3. Experimental Methods

A cross section of our device is schematically shown in Fig. 2. A 50-nm-thick TiN layer was deposited on a SiN/SiO_2/Si substrate as the bottom electrode. Electrodes were formed after the deposition of 175-nm-thick SiO_2. The SiO_2 hole was then fabricated by wet etching, and the size of the hole d_h is about 700 nm. A 50-nm-thick GST film as the phase-change layer and $TiSi_3$ as the top electrode were deposited using radio-frequency sputtering equipment (ULVAC MNS-3000-RF) at a background pressure below 5×10^{-5} Pa, a sputtering pressure of 0.2 Pa, and a radio frequency power of 100 W. $TiSi_3$ is adopted here because it has a thermal conductivity of about 10–20 W/mK,[24] much lower than that (174 W/mK)[25] of W, which is widely used as the electrode material in PCM devices. Crystallization can thus be easily controlled owing to the low heat loss by adopting an electrode material with a low thermal conductivity. Current–voltage (I–V) characteristics of the device samples were measured using a semiconductor parameter analyzer (Agilent Technologies 4155B).

4. Results and Discussion

Figure 3 illustrates the schematic concept of MLS with four resistance levels based on filament formation, crystallization, and the subsequent enlargement of the crystalline region. The device begins with an amorphous state, in which the atomic arrangement has a lack of recognizable long-range order, as shown in Fig. 3(b). The device has a high resistance R_0 because of the high resistivity of the amorphous phase. A filament is formed by applying a voltage above the threshold voltage V_{th} (corresponding to the threshold electric field E_{th}),[6,14,26] and the area of the filament is crystallized by Joule heating after the filament forms, as shown in Fig. 3(c). The formation of the narrow filament causes the first resistance drop from R_0 to R_1 because of the low resistivity of the crystallized filament. Certainly, the current mainly flows through the filament and thus the crystallized region becomes larger by Joule heating with the increasing current, as shown in Fig. 3(d). Device resistance correspondingly drops from R_1 to R_2. In the case of filament formation and crystallization, very thin layers of GST, which contact the top $TiSi_3$ layer and the underlying TiN layer, still remain in random order because high energy is necessary to make the boundary area become in an orderly array. The total region in the GST layer lying directly above the TiN layer can be completely crystallized by applying a sufficiently high current, as shown in Fig. 3(e). The device resistance finally changes from R_2 to R_3. In this work, a large ratio ($d_h/t_{GST} = 14$) of the hole diameter d_h

(700 nm) to GST thickness t_{GST} (50 nm) was adopted. Thus the electric field induced by applied electric bias reasonably concentrates in some thinner places. The filament thus forms in the concentrated electric field region. The enlargement of crystallization then takes place around the filament. Our suggested mechanism in this work is obviously different from the MLS mechanisms described in §2, especially from that based on a high-power amorphization process.

Figure 4(a) shows the shifted I–V curves of Sn ($n = 1$–8) when the current was swept between the electrodes. The current applied to the device is called the device current here, and the measured voltage across the device is called the device voltage. We first swept the device current forward from 0 to the maximum current I_{max1} of 0.2 mA and backward from 0.2–0 mA. The I–V curve corresponds to S1 in Fig. 4(a). Then, we increased the maximum current to 0.3 mA (I_{max2}) and swept the current from 0–0.3 mA and then back to 0 mA. The measured I–V curve corresponds to S2 in Fig. 4(a). Similarly, we gradually increased the maximum currents to 0.5 mA (I_{max3}), and finally to 3.5 mA (I_{max8}), and the I–V curves of S3, S4, S5, S6, S7, and S8 were measured. To clearly show these curves of Sn ($n = 1$–8), they are shifted up by $0.5 \times (n - 1)$ mA. For example, the I–V curve S2 is shifted up by 0.5 mA and the I–V curve S3 is shifted up by 1 mA. The forward sweeping is used for switching from one resistance level to the other resistance level and the backward sweeping is used for investigating the difference between the resistance levels before and after switching and the stability of the resulting resistance level. As shown in curve S1 in Fig. 4(a), current-sweeping from 0–0.2 mA did not change the resistance level at all because the forward and backward curves are almost the same, and thus the GST layer still remained completely amorphous. Current-sweeping up to 0.3 mA, i.e., above the threshold current (approximately 0.25 mA), induced a sudden switching, as shown in curve S2 in Fig. 4(a). The corresponding threshold voltage is about 1.05 V, which is much lower than that of our previous GST lateral device, 5.5 V.[4] There exists an almost linear relationship between the threshold voltage and the thickness of GST.[14,26] It is thought that the low threshold voltage is mainly caused by the reduction of the thickness (or the distance for a lateral device) between two electrodes. The first sudden switching was caused by the filament formation [corresponding to Fig. 3(c)]. The increasing maximum current from 0.3–0.5 mA led to the further resistance change, as shown in curve S3 in Fig. 4(a). For all the other curves (curves S4–S7), hysteresis characteristics are clearly seen because the forward curve is different from the backward curve. The hysteresis is caused by the gradual crystallization. For example, let us typically consider the I–V curve of S4. Crystallization did not proceed at all when the applied current was lower than the current I_{max3}. Device resistance gradually decreased owing to the promotion of crystallization during the current sweeping up to I_{max4}. Correspondingly, the I–V curve started to change with the device resistance. The crystallization did not proceed further when the applied current was swept backward to 0 mA. As we can see, the resistance level was changed by increasing the maximum currents.

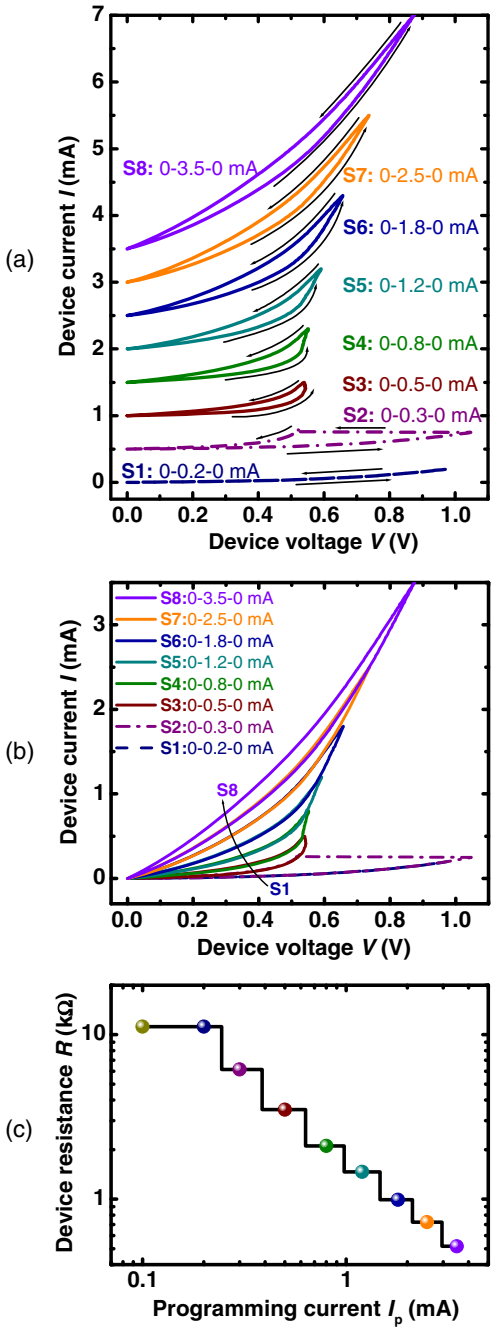

Fig. 4. (Color online) Multilevel storage in the fabricated device. (a) Shifted I–V curves when the current was swept forward from 0 mA to the programming current and backward from the programming current to 0 mA. The programming current, I_p, increases from 0.2–3.5 mA. Curve Sn ($n = 1$–8) is shifted by $0.5 \times (n - 1)$ mA. (b) I–V curves without any shift exhibit an S-shaped outline due to the resistance changes. (c) Device resistance as a function of the programming current showing eight resistance levels.

Furthermore, all of these curves are shown in Fig. 4(b) without any shift. The part of curve S3 ranging from 0 mA to the former maximum current I_{max2} 0.3 mA of curve S2 perfectly overlaps the former backward curve of S2. This means that the resulting resistance level of S2 was retained although the current was swept between 0 and 0.3 mA. Here we call the part of the curve in the forward direction the retaining part, in which there are no resistance changes. Curve S3 started to change once the applied current became

larger than the former maximum current 0.3 mA, and this part ranging from I_{max2} (0.3 mA) to I_{max3} (0.5 mA) in the forward direction set the device. We call the part of the curve in the forward direction the setting part, in which the device resistance changes. All of the curves from S2 to S8 show the same characteristics with both a retaining part and a setting part. It is very clear that the resulting resistance is very stable only if a higher current is not applied. The first sudden switching shown in curve S2 of Fig. 4(b) was caused by the filament formation, and the subsequent hysteresis characteristics in curves S3–S8 of Fig. 4(b) were created by the promotion of the crystallization, as described above.

It is clearly known that the device resistance is determined only by the applied maximum current from the above analysis and we call the applied maximum current the programming current. The device resistances read at a low current with increasing programming currents are shown in Fig. 4(c). The device resistance was 11.2 kΩ and did not change at 0.1 and 0.2 mA. The first switching resulted in a resistance drop from 11.2–6.2 kΩ at a programming current of 0.3 mA. Then, a higher programming current caused a resistance drop to 3.5 kΩ at a programming current of 0.5 mA. The resistance further drops to 2.1 kΩ by increasing the programming current to 0.8 mA. Similarly, the increasing programming current induced a decreased resistance level. The device resistance reduced to 0.5 kΩ after applying a programming current of 3.5 mA. These subsequent gradual resistance drops resulted from the enlargement of the crystalline region, as shown in Fig. 3(d). Eight distinct and stable resistance levels were created in this study, and they were induced by current-driven programming. These discrete resistance levels corresponding to crystallization regions of different sizes were determined by the programming currents. In other words, a certain programming current can induce a certain crystallization region, resulting in a certain resistance level. Here, we applied eight different programming currents for eight different resistance levels considering the data storage format in computers or other electronic devices. In this case, three bit data per cell can be realized for eight resistance levels. It is possible to obtain a desired number of resistance levels by appropriately changing the number of programming currents.

5. Conclusions

In summary, we demonstrated multilevel storage based on low-power crystallization instead of high-power amorphization using a vertical TiSi/GST/TiN PCM cell structure. The crystallization induced by Joule heating is nonvolatile, low-power, and current-driven, and allows multilevel storage. This phenomenon can be employed in practical applications to dramatically increase the memory capacity without increasing the cell size.

Acknowledgements

This work was financially supported by a Grant-in-Aid for Young Scientists (A) from the Ministry of Education, Culture, Sports, Science and Technology of Japan. We also would like to acknowledge the financial support of the Semiconductor Technology Academic Research Center (STARC) of Japan.

1) S. R. Ovshinsky: Phys. Rev. Lett. **21** (1968) 1450.
2) D. S. Chao, C. H. Lien, C. M. Lee, Y. C. Chen, J. T. Yeh, F. Chen, M. J. Chen, P. H. Yen, M. J. Kao, and M. J. Tsai: Appl. Phys. Lett. **92** (2008) 062108.
3) K. Terabe, T. Hasegawa, T. Nakayama, and M. Aono: Nature **433** (2005) 47.
4) Y. Yin, T. Noguchi, H. Ohno, and S. Hosaka: Appl. Phys. Lett. **95** (2009) 133503.
5) T. Hasegawa, N. Alpana, T. Ohno, K. Terabe, T. Tsuruoka, J. K. Gimzewski, and M. Aono: Appl. Phys. A **102** (2011) 811.
6) Y. Yin, H. Sone, and S. Hosaka: Microelectron. Eng. **84** (2007) 2901.
7) F. Rao, Z. Song, M. Zhong, L. Wu, G. Feng, B. Liu, S. Feng, and B. Chen: Jpn. J. Appl. Phys. **46** (2007) L25.
8) X. Zhou, L. Wu, Z. Song, F. Rao, Y. Cheng, C. Peng, D. Yao, S. Song, B. Liu, S. Feng, and B. Chen: Appl. Phys. Lett. **99** (2011) 032105.
9) G. Lee, J. Lee, Y. H. Song, J. C. Bea, T. Tanaka, and M. Koyanagi: Jpn. J. Appl. Phys. **50** (2011) 095001.
10) G. Zhang, W. S. Hwang, S. Lee, B. Cho, and W. J. Yoo: IEEE Trans. Electron Devices **55** (2008) 2361.
11) Y. Yin, K. Ota, T. Noguchi, H. Ohno, H. Sone, and S. Hosaka: Jpn. J. Appl. Phys. **48** (2009) 04C063.
12) S. R. Ovshinsky: Jpn. J. Appl. Phys. **43** (2004) 4695.
13) M. Liu, Z. Abid, W. Wang, X. He, Q. Liu, and W. Guan: Appl. Phys. Lett. **94** (2009) 233106.
14) M. H. R. Lankhorst, B. W. S. M. M. Ketelaars, and R. A. M. Wolters: Nat. Mater. **4** (2005) 347.
15) A. Makarov, V. Sverdlov, and S. Selberherr: J. Vac. Sci. Technol. B **29** (2011) 01AD03.
16) J. Feng, Y. F. Lai, B. W. Qiao, B. C. Cai, Y. Y. Lin, T. A. Tang, and B. Chen: Jpn. J. Appl. Phys. **46** (2007) 5724.
17) G. H. Oh, Y. L. Park, J. I. Lee, D. H. Im, J. S. Bae, D. H. Kim, D. H. Ahn, H. Horii, S. O. Park, H. S. Yoon, I. S. Park, Y. S. Ko, U. I. Chung, and J. T. Moon: Proc. Symp. VLSI Technology, 2009, p. 220.
18) Y. Gu, Z. Song, T. Zhang, B. Liu, and S. Feng: Solid-State Electron. **54** (2010) 443.
19) E. T. Kim, J. Y. Lee, and Y. T. Kim: Phys. Status Solidi: Rapid Res. Lett. **3** (2009) 103.
20) Y. C. Chen, C. T. Rettner, S. Raoux, G. W. Burr, S. H. Chen, R. M. Shelby, M. Salinga, W. P. Risk, T. D. Happ, G. M. McClelland, M. Breitwisch, A. Schrott, J. B. Philipp, M. H. Lee, R. Cheek, T. Nirschl, M. Lamorey, C. F. Chen, E. Joseph, S. Zaidi, B. Yee, H. L. Lung, R. Bergmann, and C. Lam: IEDM Tech. Dig., 2006, p. 777.
21) A. Pirovano, A. L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez: IEDM Tech. Dig., 2003, p. 699.
22) G. Bruns, P. Merkelbach, C. Schlockermann, M. Salinga, M. Wuttig, T. D. Happ, J. B. Philipp, and M. Kund: Appl. Phys. Lett. **95** (2009) 043108.
23) G. Zhang, Z. Wu, J. H. Jeong, D. S. Jeong, Y. J. Won, and B. K. Cheong: Curr. Appl. Phys. **11** (2011) e79.
24) V. S. Neshpor: J. Eng. Phys. Thermophys. **15** (1968) 750 [in Russian].
25) Y. Yin, H. Sone, and S. Hosaka: Jpn. J. Appl. Phys. **45** (2006) 6177.
26) S. R. Ovshinsky and H. Fritzsche: IEEE Trans. Electron Devices **20** (1973) 91.